REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correction to case outline dimensions. Changes to table I.	87-11-17	M. A. Frye
B	Change data hold time limits. Change conditions for reference output voltage. Change footnote 2. Add footnote to reference input resistance test. Delete compliance voltage test. Device type 01 inactive for new design, see table I footnote 4/.	89-01-09	M. A. Frye
C	Redraw. Update drawing to current requirements. Editorial changes throughout. - -drw	08-04-02	Robert M. Heber

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																				
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REV STATUS				REV			C	C	C	C	C	C	C	C	C	C	C			
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A	PREPARED BY Joseph A. Kerby	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY D. H. Johnson	
	APPROVED BY Michael A. Frye	MICROCIRCUIT, LINEAR, MICROPROCESSOR COMPATIBLE, 12-BIT D/A CONVERTER, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 87-03-19	
	REVISION LEVEL C	SIZE: A; CAGE CODE: **14933**; **5962-87801** SHEET: 1 OF 11

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-87801	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	AD567	12-bit current output D/A converter, microprocessor compatible.

1.2.2 Case outline. The case outline is as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in -line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V_{CC} to POWER GROUND	0 V dc to +18 V dc
V_{EE} to POWER GROUND	0 V dc to -18 V dc
Voltage on DAC OUT (pin 2)	-3 V dc to +12 V dc
Digital inputs (pins 10-15, 17-28) to POWER GROUND	-1.0 V dc to 7.0 V dc
V_{REF} IN to REF GND	±12 V dc
BIP OFFSET to REF GND	±12 V dc
10 V SPAN R to REF GND	±12 V dc
20 V SPAN R to REF GND	±24 V dc
V_{REF} OUT short to POWER GROUND	Continuous
Power dissipation (P_D)	1,000 mW
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA})	60°C/W

1.4 Recommended operating conditions.

Supply voltage, V_{CC}	+15 V dc
Supply voltage, V_{EE}	-15 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Relative accuracy	R_A	All bits with positive errors on; All bits with negative errors on.	1	01		±1/2	LSB
			2, 3			±3/4	
Differential nonlinearity	DNL	Major carry errors	1	01		±3/4	LSB
			2, 3			±1	
Gain error	A_E	All bits on	1	01		±0.25	%FSR
Gain temperature coefficient	TCA_E		2, 3			±30	ppm of FSR/°C
Unipolar offset error	V_{OS}	All bits off	1	01		±0.05	%FSR
Unipolar offset temperature coefficient	TCV_{OS}		2, 3			±2	ppm of FSR/°C
Bipolar zero error	B_{PZE}	MSB on, all other bits off; bipolar mode	1	01		±0.15	%FSR
Bipolar zero temperature coefficient	TCB_{PZE}		2, 3			±10	ppm of FSR/°C
Reference input resistance 2/	R_{IN}	T_A = +25°C	1	01	15	25	kΩ
Output resistance	R_{OUT}	Excluding span resister T_A = +25°C	1	01	6	10	kΩ
Reference output voltage 3/	V_{REF}	Unipolar mode, 1.1 mA external load, V_{CC} = +12 V, V_{EE} = -12 V	1, 2, 3	01	9.9	10.10	V
Output current 4/	I_{OUT}	Unipolar mode, V_{IH} = 5 V, All bits on, T_A = +25°C	1	01	-1.6	-2.4	mA
		Bipolar mode, V_{IH} = 5 V, All bits on, T_A = +25°C			±0.8	±1.2	
Power supply rejection ratio 4/	PSRR	+11.4 V ≤ V_{CC} ≤ +16.5 V T_A = +25°C	1	01		10	ppm of FSR/%
		-16.5 V ≤ V_{CC} ≤ -11.4 V T_A = +25°C				25	
Power supply current 4/	I_{CC}	V_{CC} = +16.5 V, V_{EE} = -16.5 V All bits low, T_A = +25°C	1	01		5	mA
	I_{EE}					-25	
Power dissipation 4/, 5/	P_D		1	01		495	mW

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital input high voltage 4/	V_{IH}	$T_A = +25°C$	1	01	2.0		V
Digital input low voltage	V_{IL}		1	01		0.8	V
			2, 3			0.7	
Digital input high current 4/	I_{IH}	$V_{IH} = 5.5$ V, $T_A = +25°C$	1	01		±300	µA
Digital input low current 4/	I_{IL}	$V_{IL} = 0$ V, $T_A = +25°C$	1	01		±100	µA
Functional tests		See 4.3.1c	7, 8	01			
Output current settling time	t_{SL}	See figure 4, $T_A = +25°C$ 2/, 4/	9	01		500	ns
Write pulse width	t_{WR}				100		
Data setup time	t_{DW}				50		
Data hold time	t_{DH}				10		
$\overline{CS}$ valid to end of $\overline{WR}$	t_{CW}				100		
Address valid to end of $\overline{WR}$	t_{AW}				100		

1/ $V_{CC} = +15$ V dc, $V_{EE} = -15$ V dc, 50Ω resistor pin 6 to pin 8, pins 10-15 = logic "0", $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V, unless otherwise specified.

2/ Guaranteed if not tested parameter.

3/ In subgroup 1, the reference output is loaded with 0.5 mA nominal reference current and 1.1 mA bipolar offset current, with the DAC in +10 V range, unipolar mode. In subgroups 2 and 3, only the 0.5 mA reference input current is applied. The reference must be buffered to supply external loads at elevated temperature.

4/ These parametric limits represent +25°C characterization and testing only. For these particular parameters, device type 01 does not meet the full military operating range requirements of 1.2.1 of MIL-STD-883.

5/ Power dissipation performance is checked as part of the power supply current test, I_{CC}, I_{EE}.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	BIP OFFSET
2	DAC OUT (2 mA F.S.)
3	10 V SPAN R
4	20 V SPAN R
5	REF GND
6	V_{REF} OUT
7	$+V_{CC}$
8	V_{REF} IN
9	$-V_{EE}$
10	$\overline{CS}$
11	$\overline{WR}$
12	A3
13	A2
14	A1
15	A0
16	POWER GROUND
17	DB0 (LSB)
18	DB1
19	DB2
20	DB3
21	DB4
22	DB5
23	DB6
24	DB7
25	DB8
26	DB9
27	DB10
28	DB11 (MSB)

FIGURE 1. Terminal connections.

$\overline{CS}$	$\overline{WR}$	A3	A2	A1	A0	Operation
1	X	X	X	X	X	No operation
X	1	X	X	X	X	No operation
0	0	1	1	1	0	Enable 4 LSBs of first rank
0	0	1	1	0	1	Enable 4 middle bits of first rank
0	0	1	0	1	1	Enable 4 MSBs of first rank
0	0	0	1	1	1	Loads second rank from first rank
0	0	0	0	0	0	All latches transparent

X = Don't care

FIGURE 2. Truth table.

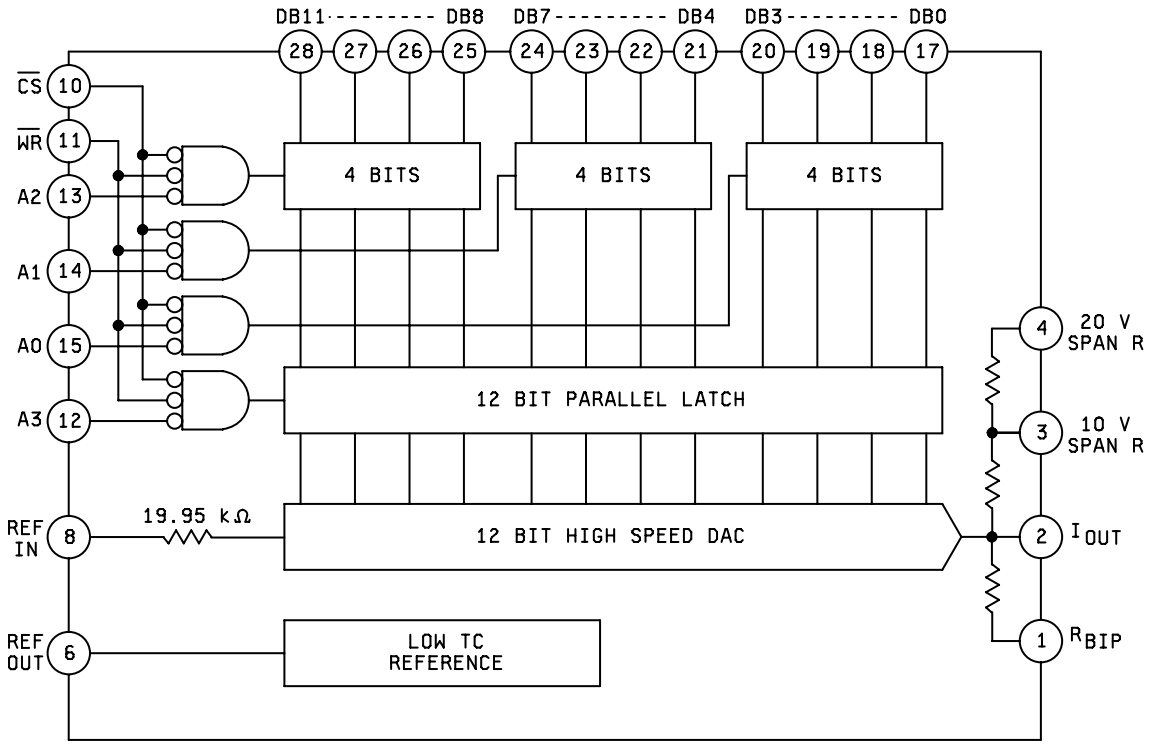

FIGURE 3. Functional block diagram.

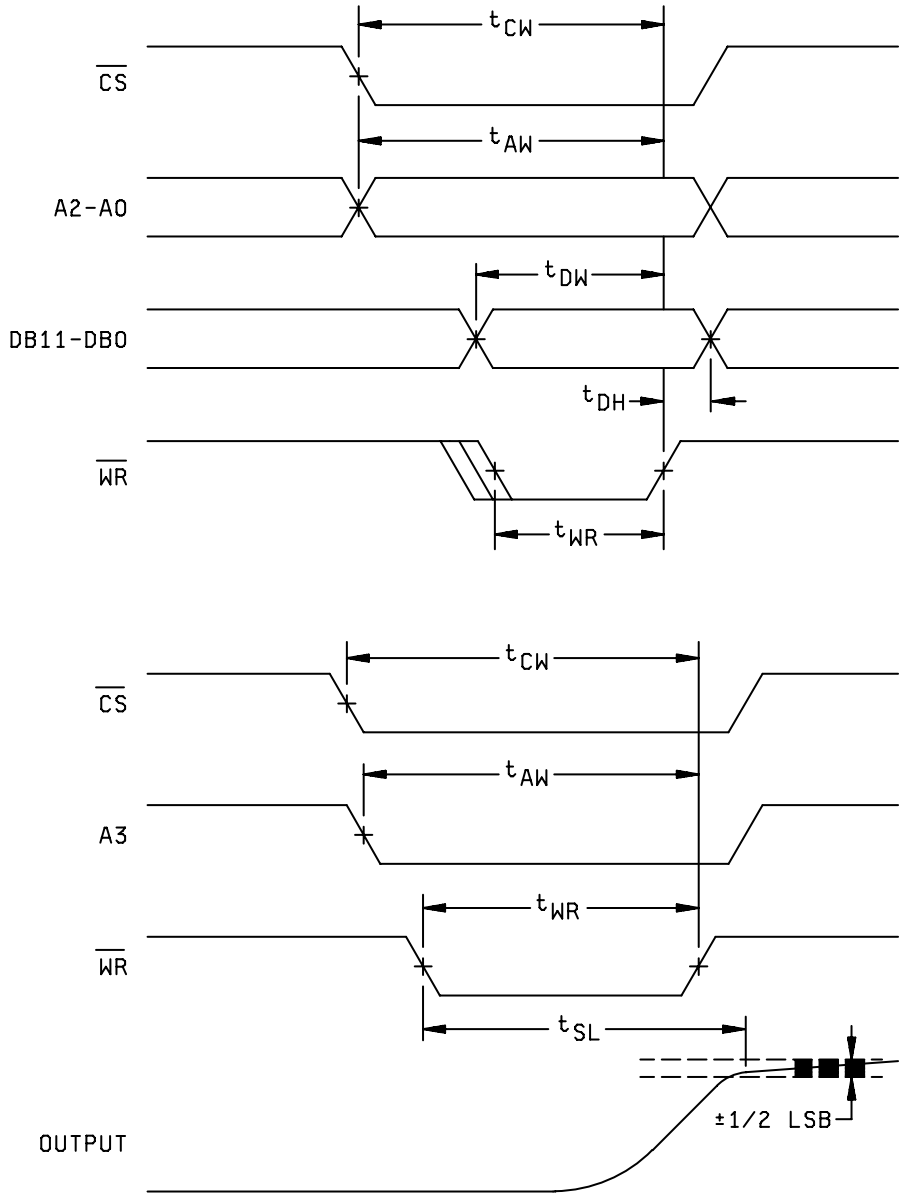

FIGURE 4. Switching waveforms.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroup 9, if not tested, shall be guaranteed to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-04-02

Approved sources of supply for SMD 5962-87801 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8780101XA	24355	AD567SD/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: 804 Woburn Street Wilmington, MA 01887-3462

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.